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(54) **A package for a semiconductor chip**

(57) A package for a semiconductor chip (14) includes as an integral part thereof a frame-shaped surround preferably comprising a multilayer ceramic capacitor (20). The chip is mounted within the frame. Conductive portions (e.g. 40) of the capacitor serve as the terminals and plates of the capacitor and as planar power and ground members for interconnecting an external power supply to the chip. By means of these planar members, power is distributed to the chip in a low-impedance, substantially transient-free manner without utilizing any of the multiple signal leads emanating from the package. Moreover, the signal leads (21—33) are separated from the ground plane by a low-dielectric-constant material (42). As a result, the signal leads are minimally loaded and are characterised by a relatively constant impedance selected to optimise signal transfer to and from the chip.

FIG. 1

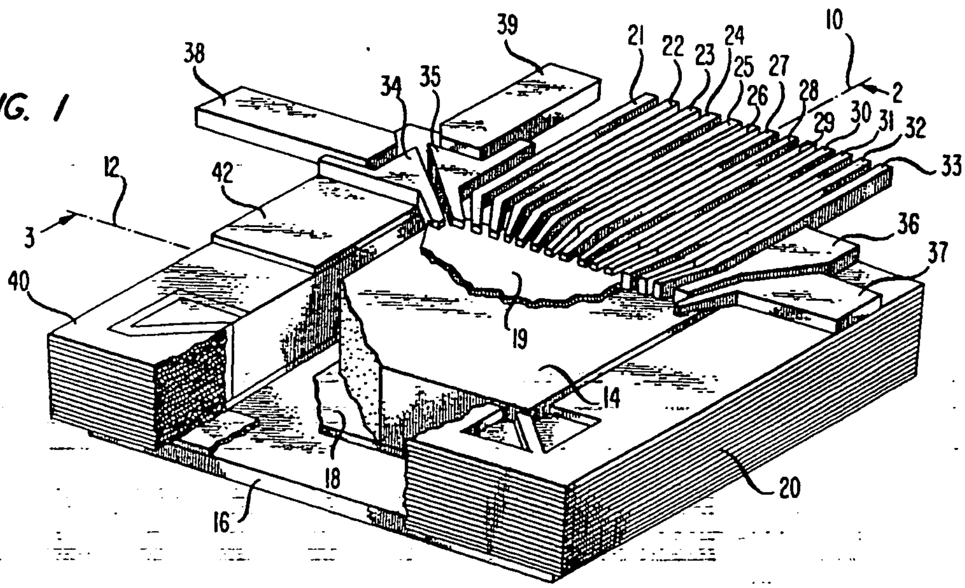

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FIG. 1

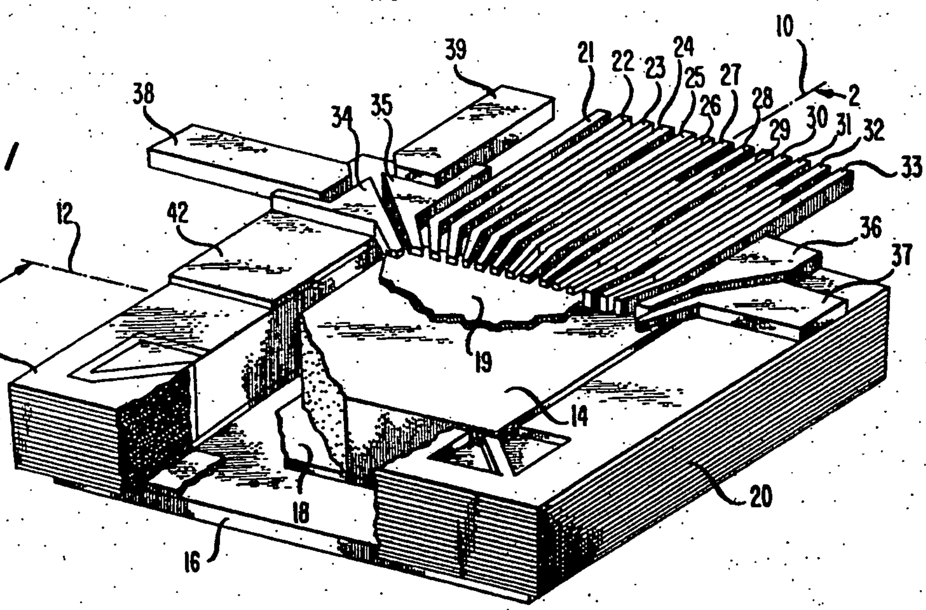


FIG. 2

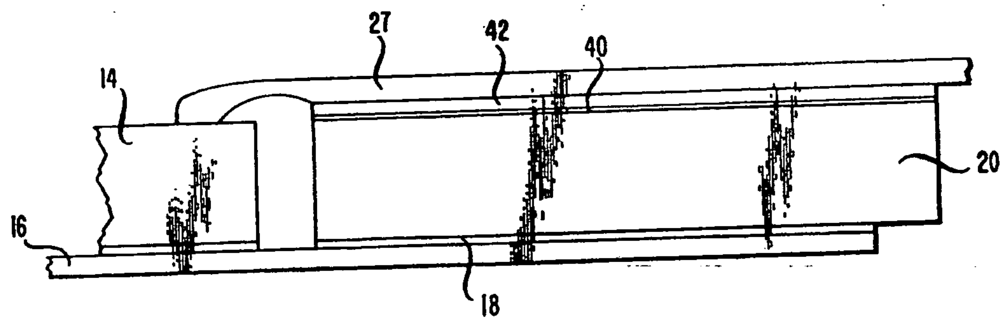
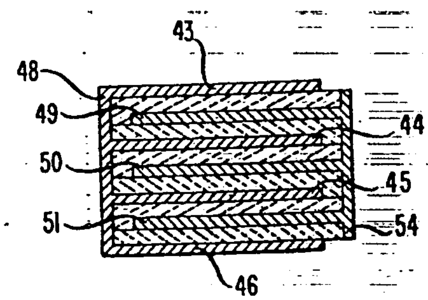


FIG. 3



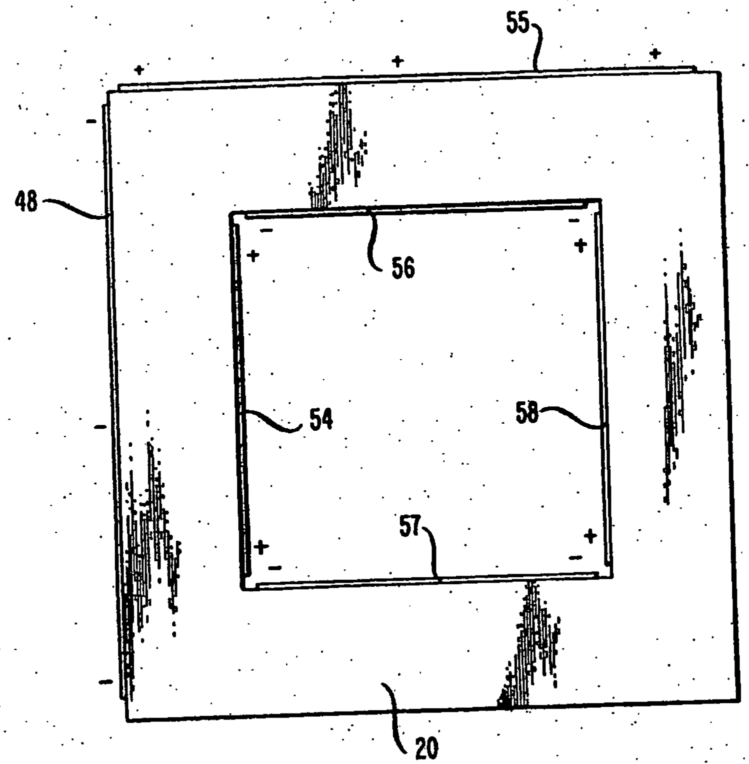


FIG. 4

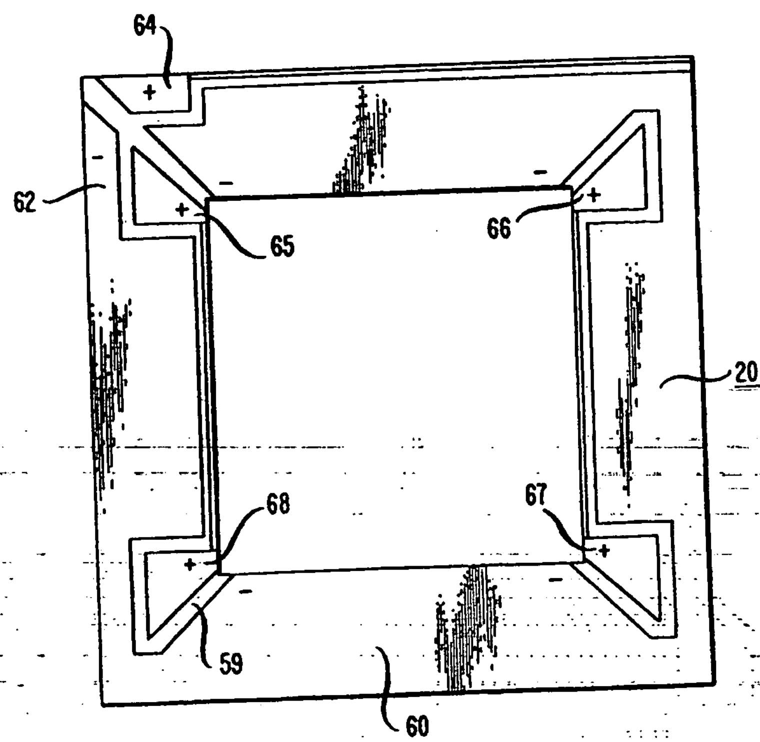


FIG. 5

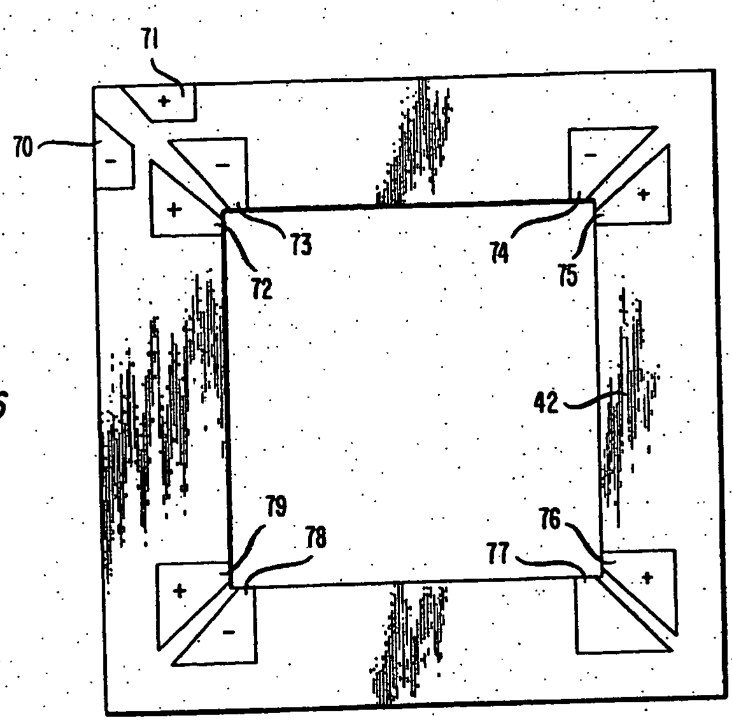


FIG. 6

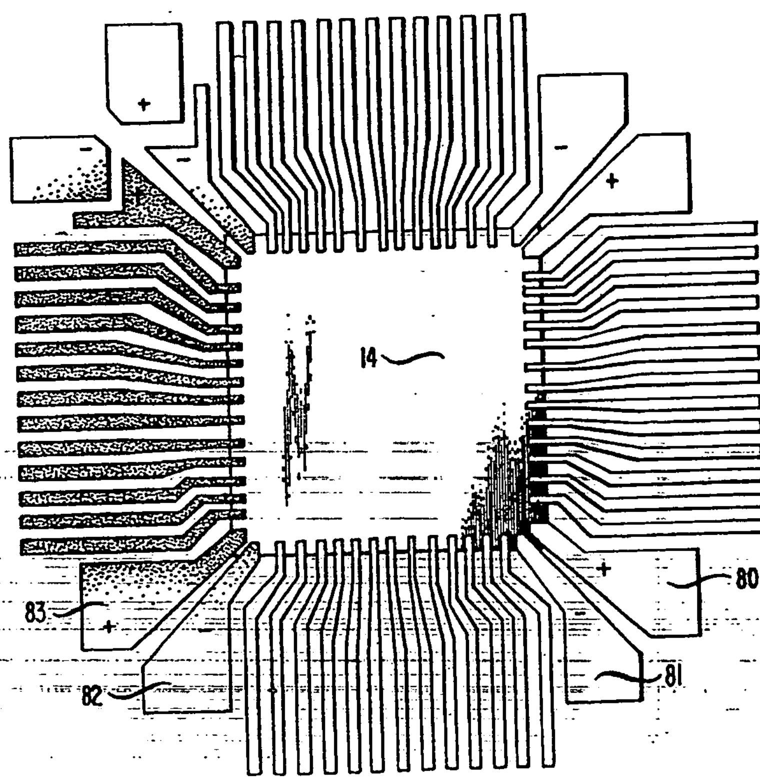


FIG. 7

SPECIFICATION

A package for a semiconductor chip

This invention relates to semiconductor chips and, more particularly, to a package structure for housing and establishing electrical connections to such a chip.

Various designs for packaging semiconductor chips are known. Some of these designs provide adequate mechanical, environmental and thermal protection for the housed chip. But, with respect to establishing signal and power connections to the chip, these package designs typically treat signal interconnection and power distribution to the chip as being basically the same. As a result of this standard design approach, conventional packages suffer from the disadvantage that the power supplied to the chip may include undesirable switching transients. This is particularly true if relatively large currents must be switched and delivered to the chip in a high-speed manner. In such cases, the presence of even small inductances in the power supply distribution network, even within the chip package, can generate significant spurious voltage signals. Such signals can, of course, deleteriously affect the performance of the chip.

To minimise the impedance, especially the inductance, of the distribution network that supplies power to the chip, it is standard practice in a conventional high-performance package design to utilize multiple ones of the package leads as power and ground connections. This approach tends to reduce inductance and thereby reduce the magnitude of spurious or transient signals that occur in the power distribution network. But one penalty of this approach is that a relatively large number of pins or leads of the package are thereby made unavailable for signal transfer purposes. In some cases, this may in turn necessitate redesign of the package to provide a physically larger unit with additional signal leads. Such a redesign, however, clearly runs counter to the desired goal of making the packaged chips as small as possible.

Additionally, a separate by-pass capacitor element is often utilized in the distribution network that supplies power to an integrated circuit chip. Spurious noise signals arising from switching transients are shunted by the by-pass capacitor element and thereby kept from being applied to the chip. Moreover, the capacitor acts as a local reservoir of energy for current surges drawn by the chip. But, even if such a capacitor element is positioned physically close to its associated chip on a mounting board, inductance in the leads connecting the element to the chip can be the basis for generating significant spurious voltages in the connecting leads. These voltages are "seen" only at the chip itself. Moreover, the bypass capacitors included in a microelectronic assembly can occupy a significant part of the available area on the mounting board. As the trend to smaller and smaller assemblies continues, it would obviously be desirable to reduce the board area occupied by by-pass capacitors.

Accordingly, considerable effort has been directed at trying to design improved packages for semiconductor chips. In particular, much effort has been directed at trying to provide small-size packaged chips exhibiting high-performance electrical characteristics.

According to the present invention there is provided a package comprising a body defining an interior cavity, adapted for mounting of a semiconductor chip with conductive pads thereon, wherein planar ground and power members are formed in parallel planes in the body, and the members have outer peripheral portions linkable to an external power supply, and inner peripheral portions connectable to the conductive pads of the semiconductor chip when mounted.

An embodiment of the invention provides an improved package for a semiconductor chip. More specifically, there is provided a packaged chip to which power is supplied in a substantially transient-free manner and to and from which signals are transferred in a particularly effective way. Moreover, there is provided a power supply by-pass capacitor for the chip in as compact and space-saving a manner as possible.

One embodiment of the invention provides a package for a semiconductor chip including planar power and ground members. Additionally, the package includes multiple signal leads extending therefrom. By means of the planar members, power is distributed to the chip from an external power supply. Significantly, this is done in a low-impedance substantially transient-free manner.

To minimise inductance, both of the planar power and ground members are designed to be as large in area as possible. Moreover, the planar members are formed in the package in closely spaced-apart parallel planes. Electrical connections extend from the planar members to a common interconnection level of the package.

Advantageously, the signal leads are separated from the ground plane of the package by a low-dielectric-constant material. As a result, the signal leads are minimally loaded and are characterised by a relatively constant impedance selected to optimise signal transfer to and from the chip.

Moreover, in one particular illustrative embodiment of the principles of the present invention, a power supply bypass capacitor element is advantageously included in the chip package as an integral part thereof.

More specifically, one particular illustrative embodiment comprises a frame-shaped capacitor element that constitutes an integral part of the package. The chip is mounted within a recess defined by the frame-shaped element. Conductive surface portions formed on the capacitor element serve as terminals of the element and as planar power and ground members for interconnecting an external power supply to the chip. Power supply terminal members connected to the planar

members emanate from the package. Link members connect the power and ground members to the chip. Additionally, an insulating layer is formed on the planar ground member. Multiple signal leads extend from the package. These leads lie on the insulating layer and are connected to the chip.

A complete understanding of the present invention may be gained from a consideration of the following detailed description presented hereinbelow in connection with the accompanying drawings, in which:

Fig. 1 is a perspective view, partially broken away, of a specific illustrative semiconductor chip package made in accordance with one embodiment of the present invention;

Fig. 2 is a cross-sectional depiction at line 10 of Fig. 1 as viewed in the direction of arrow 2;

Fig. 3 is a cross-sectional representation at line 12 of Fig. 1 as viewed in the direction of arrow 3;

Fig. 4, which is a top view of the capacitor element included in Fig. 1, depicts side-metallised portions thereof;

Fig. 5 is a top view of the metallic pattern formed on top of the capacitor element;

Fig. 6 is a top view of an insulating layer formed on top of the metallic pattern of Fig. 5; and

Fig. 7 is a top view of the leadframe and chip shown in Fig. 1.

In Fig. 1, a conventional semiconductor chip 14 is shown mounted on a conductive plate 16 that constitutes the base member of a package for the chip. The plate 16, made, for example, of aluminum, serves as a heat sink for the depicted assembly. By way of example, the chip comprises a standard high-speed very-largescale-integrated circuit of the metal-oxide-semiconductor type. Illustratively, the bottom side of the chip 14 is bonded to the plate 16 by a layer 18 of conductive epoxy cement.

A frame-shaped element 20 surrounds the chip 14 of Fig. 1. The element 20 is also bonded to the plate 16 by means of the conductive epoxy cement layer 18. In one specific illustrative embodiment of the invention, the frame-shaped element 20, which serves as a integral part of the depicted package, comprises a by-pass capacitor.

In other embodiments of the principles of the present invention, the frame-shaped element 20 is not a capacitor but designed instead simply to be a part of the housing for the chip 14. The main emphasis herein will be directed to an embodiment in which the element 20 is a capacitor. In such an embodiment, which constitutes a particularly compact and advantageous version of applicant's invention, the closely spaced-apart plates of the capacitor itself constitute the parallel-plane-disposed power and ground members of applicant's low-inductance power distribution network.

The capacitor element 20 of Fig. 1 is formed, for example, by punching a conventional multi-layer sheet of metallized layers of ceramic. Such multilayers ceramic sheets are known in the art and commercially available. Further details of the structure of the element 20 will be set forth below in connection with the description of Fig. 3.

Advantageously, multiple connections to the chip 14 are made thereto in a standard tape-automated-bonding operation before the chip is positioned within the package shown in Fig. 1. In that operation, multiple pads on the top of the chip are simultaneously connected to a conductive foil lead-frame, in a manner well known in the art. The lead-frame-supported chip 14 is then mounted in the depicted package. Subsequently, the lead-frame is trimmed. Additionally, a layer 19 of protective material, such as standard room-temperature-vulcanising rubber, is advantageously applied to the top surface of the chip 14, as indicated in Fig. 1.

A portion of the trimmed lead-frame is shown in Fig. 1. The depicted portion comprises signal leads 21 through 33 whose free or outer ends extend beyond one outer edge of the package. The other or inner ends of these leads are respectively electrically connected to various points of the integrated circuit formed on the chip 14. Additionally, the depicted portion comprises link members 34 to 37. The inner ends of the members 34 to 37 are respectively connected to various power and ground pads on the chip 14. Outer regions of these link members are connected to planar power and ground members formed on surfaces of the capacitor element 20, as will be specified in detail later below.

Furthermore, in the preferred embodiments, the trimmed lead-frame shown in Fig. 1 also includes power and ground terminal members 38 and 39. The inner ends of these members 38, 39 are respectively connected to the planar power and ground line members 34, 35 formed on and within the capacitor element 20. The outer or free ends of the members 38 and 39 extend beyond outer edges of the package. These outer ends constitute terminal members for connecting the packaged chip to an external power supply.

In Fig. 1, only one group of thirteen signal leads 21 to 33 extending beyond one edge of the package are explicitly shown. But it is to be understood that such a package typically includes three other identical groups of signal leads respectively extending beyond the other three edges of the package. Additionally, the package also typically includes two other pairs of link members respectively disposed adjacent to the other two inner corners of the capacitor element 20. (These other signal leads and link members will be specifically identified below in connection with the description of Fig. 7.)

The upper most conductive plate 40 of the capacitor element 20 shown in Fig. 1 constitutes a planar ground member. An insulating layer 42 made, for example of a polyimide material is deposited on top of the ground member 40. In turn, all of the signal leads (such as the leads 21 through 33) include portions that rest directly on top of the insulating layer 42. In one specific illustrative embodiment, in which the width of

each signal lead is about 100 micrometers, the thickness of each signal lead is 50-to-100 micrometers and the thickness of the layer 42 is 50-to-100 micrometers, the characteristic impedance of the signal leads is thereby established at about 50-to-80 ohms.

Fig. 2 shows the conductive signal lead 27 of the packaged chip of Fig. 1. The lead 27 is disposed on the insulating layer 42 that overlies the planar ground member 40. As indicated above, the member 40 is the top conductive plate of the capacitor element 20. Portions of the chip 14, the conductive bonding layer 18 and the base plate 16 are also indicated in Fig. 2. If desired, a thin nonconductive bonding layer (not shown) may be interposed between the lead 27 and the insulating layer 42 to impart additional mechanical stability to the assembly. Alternatively, the dielectric layer 42 may itself be an adhesive material.

Fig. 3, which is a cross-sectional representation of the capacitor element 20, indicates the multilayered structure thereof. The element 20 comprises alternating layers of metal and ceramic. Metallic layers 43 to 46 are interconnected by side metallisation 48. Top metallic layer 43 constitutes the ground plane 40 shown in Fig. 1. Accordingly, in this particular illustrative embodiment, the bottom metallic layer 46 that rests in contact with the base plate 16 (Fig. 1) is also intended to be grounded.

By means of power supply terminal member 38 (Fig. 1), the ground (or relatively negative) terminal of an external direct-current power supply is connected to the layers 43 through 46 and to the side metallisation 48 shown in Fig. 3. The particular manner in which this is done within the package assembly will be specified in more detail below.

Metallic layers 49 through 51 shown in Fig. 3 are interconnected by side metallisation 54. The side portion 54 is intended to be connected to the positive terminal of an external direct-current power supply. This is done by establishing an electrical connection within the package assembly between the metallisation 54 and power supply terminal member 39, as will be specified in more detail below.

Fig. 3 shows two of the side metallisations formed on the capacitor element 20. These metallisations 48 and 54 are schematically represented in Fig. 4 and identified there with the same reference numerals utilised therefore in Fig. 3. Moreover, in Fig. 4, these metallisations 48 and 54 are designated with negative and positive signs to indicate to which respective terminals of the external power supply they are intended to be connected. Furthermore, in the embodiment, additional similar side metallisations are formed on the element 20. These additional metallisations 55 to 58 are shown in Fig. 4 and are also marked with positive and negative signs to indicate their interconnection pattern.

It is evident from Fig. 4 that energy from an external power supply enters the capacitor element 20 at the outside edges of the element. Connections for the power supply are made to those edges by means of the terminal members 38 and 39 (Fig. 1). In turn, energy is delivered from the capacitor element to the associated chip along the inner edges of the element via short connections to the chip contained therein. In that way, the inductances included in the input and output circuit paths connected to the capacitor element 20 are minimised.

Fig. 5 shows the metallisation pattern printed or otherwise formed in a standard manner on the capacitor element 20 on top of the uppermost ceramic layer 59 thereof. A major part 60 of the pattern comprises the aforespecified ground plane (designated with a negative sign). The part 60 is electrically connected to the side metallisations 48, 56 and 57 represented in Fig. 4. Illustratively, the power supply terminal member 38 (Fig. 1) is designed to contact end portion 62 of the part 60.

Also formed on top of the uppermost ceramic layer 59 (Fig 5) of the capacitor element 20 are conductive regions 64 to 68 (each marked with a positive sign). The region 64 is electrically connected to the side metallisation 55 of Fig. 4; the regions 65 and 68 are connected to the side metallisation 54 of Fig. 4; and the regions 66 and 67 are connected to the side metallisation 58 of Fig. 4.

The power supply terminal member 39 (Fig. 1) is designed to contact the conductive region 64 of Fig. 5. In that way, the positive side of the external power supply is connected to the capacitor element 20.

As indicated in Fig. 5, each of the four inner corners of the metallisation pattern formed on top of the capacitor element 20 includes positive and negative regions. By means of link members, interconnections are made between these regions and conductive pads on the chip contained within the depicted framework. Four such link members designated 34 to 37 are shown in Fig. 1.

In the aforespecified illustrative embodiment, the link member pairs are shown at the corners of the chip. But it is to be understood that these link members may be located anywhere around the periphery of the inside edge of the capacitor element 20 if appropriate electrical connections to the positive (power) metallization are made by conductive patterns and/or conductive vias through the uppermost ceramic layer of the capacitor element.

Fig. 6 shows the pattern of the insulating layer 42 formed on top of the planar ground member 40 of Fig. 1. Openings 70 to 79 in the layer 42 provide access therethrough to selected portions of the underlying metallisation pattern shown in Fig. 5. By means of conductive epoxy cement or by any other standard conductive attachment technique, electrical connections are established between the overlying metallisation pattern shown in Fig. 5. By means of conductive epoxy cement or by any other standard conductive

attachment technique, electrical connections are established between the overlying lead-frame (Fig. 1) and the metallisation portions directly underlying the openings 70 to 79.

Fig. 7 is a top view of the particular illustrative package chip of Fig. 1. All fifty-two signal leads connected to the chip 14 are explicitly shown in Fig. 7. Moreover, the previously specified power supply terminal members 38 and 39 and the link members 34 to 37 associated with two corners of the chip 14 are also shown in Fig. 7. Further, four additional link members 80 to 83 associated with the other two corners of the chip 14 are also depicted in Fig. 7. By means of these eight link members, power is distributed from the inner corners of the aforedescribed capacitor element 20 to the four corners of the chip 14. And, by means of the depicted signal leads and the power supply terminal members 38 and 39, the packaged chip can be physically secured and electrically connected to a standard mounting board, in a manner well known in the art.

Numerous modifications and alternatives of the embodiment may be devised by those skilled in the art. For example, although primary emphasis herein has been directed to a package that includes as an integral part thereof a frame-like capacitor element, it is to be understood, as stated earlier above, that in some embodiments of this invention the frame-like member is not fabricated to be a capacitor but designed instead simply to be a part of the housing for the associated chip. In those embodiments also, planar power and ground members, suitably insulated from each other, are formed on and within portions of the frame-like member so as to minimise power-ground loop inductance. In such an embodiment, the ground member could be a top planar portion such as the member 40 of Fig. 1, and the power member could be another planar portion within the frame 20 below the member 40. Suitable electrical connections from the power member to the lead-frame level of the package are made by vias and/or surface conductive patterns, in a standard manner known in the art.

Furthermore, in those cases in which the frame-shaped element 20 is not a capacitor, the planar power and ground members may be formed in some other element of the package. For example, the base plate member 16 of Fig. 1 may be made of an insulating material having conductive power and ground members formed therein in closely spaced-apart parallel planes. Electrical connections would extend from those members to the lead-frame of the package.

Claims

1. A package comprising a body defining an interior cavity, adapted for mounting of a semiconductor chip with conductive pads thereon, wherein planar ground and power members are formed in parallel planes in the body, and the members have outer peripheral portions linkable to an external power supply, and inner peripheral portions connectible to the conductive pads of the semiconductor chip when mounted.

2. A package in accordance with claim 1, wherein link members are provided for connecting the inner peripheral portions of the planar ground and power members with the semiconductor chip.

3. A package in accordance with claims 1 or 2, wherein power supply members are provided for connecting the outer peripheral portions of the ground and power members to an external power supply.

4. A package in accordance with claim 1, 2 or 3 wherein an insulating layer is provided on a selected portion of the ground and power members.

5. A semiconductor package in accordance with claim 4, wherein multiple signal paths are provided having inner ends respectively connected to selected ones of the pads on the chip and having outer ends that serve as signal terminal members, and that a portion of each of the signal paths extends over the insulating layer.

6. A package in accordance with any one of claims 1 to 5, wherein portions of the planar ground and power members are formed on surface portions of the body farthest removed from the chip and portions of the planar ground and power members are formed on surface portions of the body proximate the main surface of the chip.

7. A package in accordance with claim 6, wherein the power supply members are respectively connected to the farthest-removed portions and the link members are connected to the proximate portions.

8. A package in accordance with any one of claims 1 to 7, wherein the body member comprises a capacitor element and the planar ground and power members constitute the terminals and plates of the element.

9. A package in accordance with claim 8, wherein the element comprises a frame-shaped multilayer metallized ceramic capacitor.

10. A semiconductor package in accordance with claim 6, 7 or 8, wherein the link members the power supply members and the signal paths constitute parts of an integral lead-frame assembly, and the link members and the inner ends of the signal paths are connected to pads on the chip in a tape-automated-bonding operation before the chip is mounted in the cavity.

11. A package for a semicondcutor chip, substantially as hereinbefore described with reference to the accompanying drawings.

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